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| 10/828,390 | 04/19/2004 | Lee W. Atkinson | 200314319-1 | 4831 |

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

| EXAMINER | |
|---|---|
| WANG, ALBERT C | |
| **ART UNIT** | **PAPER NUMBER** |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/828,390 | ATKINSON, LEE W. | |
| | Examiner | Art Unit | |
| | Albert Wang | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office action is responsive to the amendment filed 14 March 2007.

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 13 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Laboy et al., U.S. Patent No. 6,442,652 (hereinafter "Laboy").

As per claim 1, Laboy teaches a method of conserving power in a computer, comprising:

measuring a processor load (fig. 3, step 301; col. 5, lines 4-7);

configuring the computer, based on the processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded (figs. 2 & 3; col. 4, lines 35-55; col. 5, lines 4-30).

As per claim 13, Soltis teaches a computer, comprising:

means for measuring a processor load (fig. 3, step 301; col. 5, lines 4-7); and

means for deciding, based on the processor load, whether to enable speculative execution (figs. 2 & 3; col. 4, lines 35-55; col. 5, lines 4-30).

As per claim 17, Soltis teaches a computer that configures itself, based on a processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded (figs. 2 & 3; col. 4, lines 35-55; col. 5, lines 4-30).

5. Claims 1-3, 13 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Soltis, Jr. et al. (hereinafter "Soltis").

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, Soltis teaches a method of conserving power in a computer, comprising:

measuring a processor load (fig. 2, step 204; col. 5, lines 35-37 & 56-58);

configuring the computer, based on the processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded (fig. 3; col. 4, lines 48-67; col. 5, lines 9-17 & 59-67).

As per claim 2, Soltis teaches the method of claim 1, wherein configuring the computer comprises configuring a battery-powered computer (col. 1, lines 59-67).

As per claim 3, Soltis teaches the method of claim 1, wherein measuring the processor load further comprises measuring a cache hit rate (col. 2, lines 8-13; col. 5, lines 56-58).

As per claim 13, Soltis teaches a computer, comprising:

means for measuring a processor load (fig. 2, step 204; col. 5, lines 35-37 & 56-58); and

means for deciding, based on the processor load, whether to enable speculative execution (fig. 3; col. 4, lines 48-67; col. 5, lines 9-17 & 59-67).

As per claim 17, Soltis teaches a computer that configures itself, based on a processor load, so that a lesser amount of speculative execution is enabled when the processor is lightly loaded than is enabled when the processor is heavily loaded (figs. 2 & 3; col. 4, lines 48-67; col. 5, lines 9-17, 35-37 & 56-67).

As per claim 18, Soltis teaches the computer of claim 17, wherein the computer is battery-powered (col. 1, lines 59-67).

As per claim 19, Soltis teaches the computer of claim 17, wherein the processor load is measured by measuring a cache hit rate (col. 2, lines 8-13; col. 5, lines 56-58).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 12, 13, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menezes et al., U.S. Patent No 6,845,456 (hereinafter "Menezes"), in view of Mittal et al., U.S. Patent No. 5,719,800 (hereinafter "Mittal").

As per claim 1, Menezes teaches a method of conserving power in a computer, comprising:

measuring a processor load (fig. 2, step 201);

configuring the computer, based on the processor load, to decrease the performance state when the processor is lightly loaded than is enabled when the processor is heavily loaded (col. 4, lines 46-66).

Menezes does not expressly teach enabling a lesser amount of speculative execution as a means of decreasing the performance state. Mittal teaches that speculative execution consumes power (col. 2, lines 25-34) and that enabling a lesser amount of speculative execution is a means of decreasing performance to reduce power consumption (col. 11, lines 21-33 & 54-62). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Mittal's teachings to Menezes method, as decreasing the amount of speculative execution is a well known means to reduce power consumption.

As per claim 2, Menezes teaches the method of claim 1, wherein configuring the computer comprises configuring a battery-powered computer (col. 6, lines 13-25).

As per claim 12, Mittal teaches the method of claim 1, further comprising disabling branch prediction when the processor is lightly loaded (col. 7, line 66 – col. 8, line 11).

As per claim 13, Menezes teaches a computer, comprising:

means for measuring a processor load (fig. 2, step 201); and

means for deciding, based on the processor load, whether to decrease the performance state (col. 4, lines 46-66).

Menezes does not expressly teach enabling a lesser amount of speculative execution as a means of decreasing the performance state. Mittal teaches that speculative execution consumes power (col. 2, lines 25-34) and that enabling a lesser amount of speculative execution is a means of decreasing performance to reduce power consumption (col. 11, lines 21-33 & 54-62). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Mittal's teachings to Menezes method, as decreasing the amount of speculative execution is a well known means to reduce power consumption.

As per claim 14, Mittal teaches the computer of claim 13, further comprising means for adjusting the criteria upon which a decision is made whether to enable speculative execution so that a greater amount of speculative execution is enabled (col. 11, lines 21-33 & 54-62).

As per claim 17, Menezes teaches a computer that configures itself, based on a processor load, so that the performance state is decreased when the processor is lightly loaded than is enabled when the processor is heavily loaded (fig. 2; col. 4, lines 46-66).

As per claim 18, Menezes teaches the computer of claim 17, wherein the computer is battery-powered (col. 6, lines 13-25).

8. Claims 3-6 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menezes/Mittal, as applied to claims 1 and 17 above, and further in view of Atkinson, U.S. Patent No. 5,625,826.

As per claims 3, 5, 6 and 19-22, Menezes does not expressly teach measuring the processor load further comprises measuring a cache hit rate. Atkinson teaches measuring the processor load may alternatively comprise measuring a cache hit rate, measuring the occurrence of memory page misses, and measuring the occurrence of input/output write cycles (col. 2, lines 37-51; col. 6, line 51 – col. 7, line 33). At the time of the invention, it would have been obvious to one of ordinary skill in the art to Atkinson's teachings to Menezes method, as the Atkinson teaches measuring processor load using reliable alternative means (Atkinson, col. 2, lines 25-35).

As per claim 4, Menezes teaches assigning a first value to the processor load in response to a first measurement, and assigning a second value to the processor load, higher than the first, in response to a second measurement, lower than the first (col. 4, lines 46-66).

9. Claims 7-11, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menezes/Mittal, as applied to claims 1 and 13 above, and further in view of Bittel et al., U.S. Patent No. 6,820,173 (hereinafter "Bittel").

As per claims 7 and 16, Mittal does not expressly teach utilizing branch predictions as speculative execution. Bittel teaches that branch prediction is one of numerous forms of speculative execution (col. 5, line 54 – col. 6, line 3). At the time of the invention in view of Bittel, it would have been obvious to one of ordinary skill in the art that speculative execution may take the form of branch prediction, as branch prediction is a well known form of speculative

execution. Bittel further teaches that the amount of speculative execution may be controlled by selectively setting the branch confidence threshold value (col. 5, line 54 – col. 6, line 3; col. 7, lines 47-58).

As per claims 8 and 15, Bittel teaches the method of claim 7, further comprising: assigning to a branch instruction a confidence level that the branch will be predicted correctly; comparing the confidence level with the branch confidence threshold; and deciding based on the result of the comparison whether to enable speculative execution (col. 3, lines 38-50; col. 6, lines 55-62).

As per claims 9 and 10, Mittal teaches that parameters may be set either by software or by hardware (col. 9, line 50 – col. 10, lines 16)

As per claim 11, Bittel teaches the confidence level that the branch will be predicted corrected is based on past behavior of the branch instruction (col. 5, lines 31-41; col. 6, lines 45-54).

10. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menezes et al., U.S. Patent No 6,845,456 (hereinafter "Menezes"), in view of Mittal et al., U.S. Patent No. 5,719,800 (hereinafter "Mittal"), and Bittel et al., U.S. Patent No. 6,820,173 (hereinafter "Bittel").

As per claim 23, Menezes teaches a computer method, comprising:

computing, from the measured processor load, whether to decrease the performance state (fig. 2; col. 4, lines 46-66).

Menezes does not expressly teach enabling a lesser amount of speculative execution as a means of decreasing the performance state. Mittal teaches that speculative execution consumes power (col. 2, lines 25-34) and that enabling a lesser amount of speculative execution is a means of decreasing performance to reduce power consumption (col. 11, lines 21-33 & 54-62). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Mittal's teachings to Menezes method, as decreasing the amount of speculative execution is a well known means to reduce power consumption.

Mittal does not expressly teach utilizing branch predictions as speculative execution. Bittel teaches that branch prediction is one of numerous forms of speculative execution (col. 5, line 54 – col. 6, line 3). At the time of the invention in view of Bittel, it would have been obvious to one of ordinary skill in the art that speculative execution may take the form of branch prediction, as branch prediction is a well known form of speculative execution. Bittel further teaches that the amount of speculative execution may be controlled by selectively setting the branch confidence threshold value (col. 5, line 54 – col. 6, line 3; col. 7, lines 47-58).

Bittel teaches further assigning to a branch instruction a confidence level that the branch will be predicted correctly; comparing the confidence level with the branch confidence threshold; and deciding based on the result of the comparison whether to enable speculative execution (col. 3, lines 38-50; col. 6, lines 55-62).

As software and hardware are interchangeable for performing many functions (e.g. see Mittal, col. 9, line 50 – col. 10, line 16), it would have been obvious that the above steps may be implemented in logic.

As per claim 24, Bittel teaches assigning a confidence level to the branch instruction further comprises a branch history counter that has a value reflecting the number of times execution of the branch instruction has previously resulted in a branch taken, and wherein the confidence level is derived from the branch history counter (col. 5, lines 31-41; col. 6, lines 45-54).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AW

CHUN CAO
PRIMARY EXAMINER